2001, May 15, 2002, June 27, 2003, and September 28, 2004. However, the Applicants have not received acknowledgment of the Information Disclosure Statement filed on May 22, 2002 (received by OIPE June 3, 2002). The Advisory Action implies that the Applicants have not provided "a filing receipt showing the prior submission of the IDS form" (page 2, Paper No. 093005). However, along with the *After Final Response* filed September 1, 2005, the Applicants submitted a copy of the Information Disclosure Statement filed on May 22, 2002, together with a copy of the post card confirming receipt of the IDS at OIPE on June 3, 2002. As a courtesy to the Examiner, the Applicants again submit a copy of the post card confirming receipt of the IDS at OIPE on June 3, 2002. It is respectfully submitted that the above-referenced Information Disclosure Statement was properly filed on May 22, 2002, and should be accorded its filing date for the purposes of consideration and compliance with 37 CFR §§ 1.97 and 1.98. The Applicants respectfully request that the Examiner provide an initialed copy of the Form PTO-1449 evidencing consideration of this Information Disclosure Statement.

Claims 23-32 are pending in the present application, of which claim 23 is independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

Please incorporate by reference the arguments presented in the *After Final Response* filed September 1, 2005, and the *Preliminary Amendment under 37 CFR § 1.607 and Notification of Other Amendments Under 37 § 1.607 in Related Patent Applications* filed April 30, 1997.

The Advisory Action implies that the Applicants have not tailored their arguments to the present application (page 2, Paper No. 093005). Details as to why an interference should be declared between the present application and U.S. Patent No. 5,561,075 to Nakazawa are presented in detail in the *Preliminary Amendment*.

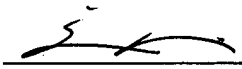
The Advisory Action asserts that "arguments submitted for an interference proceeding for a divisional do not constitute proper prosecution of the current Application and fail to specifically identify where the missing elements are in the current

application" (Id.). Although it is not exactly clear what issue concerns the Examiner, it appears the Examiner may be taking issue with the header used on a chart that accompanied the *Preliminary Amendment*, such header identifying parent application Serial No. 08/504,225. The Applicants previously explained that the present specification is identical to the specification in the parent application, and that the descriptions of support for the claims in the present specification are equally applicable to the present specification. However, for some reason, this explanation was not deemed sufficient by the Examiner. In order to clarify the matter, the Applicants herein submit a chart showing support in the present application Serial No. 08/841,644 for each of the claims of the present application, which were substantially copied from U.S. Patent No. 5,561,075 to Nakazawa, for the purposes of provoking an interference with U.S. Patent No. 5,561,075 to Nakazawa (as noted previously, claims 23, 24 and 29-32 are exactly the same as claims 1, 2 and 9-12 of Nakazawa '075; claims 25-28 are generally related to claims 3 and 6-8 of Nakazawa '075).

For the reasons noted in detail in the above-referenced *Preliminary Amendment*, the Applicants respectfully request that they be designated senior party in a declaration of interference with respect to U.S. Patent No. 5,561,075 to Nakazawa.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/841,644
23. A method of manufacturing an active matrix panel in which data signals are supplied to liquid crystal layers through a plurality of thin film transistors arranged in a matrix of pixels, gate lines and data lines being coupled to each thin film transistor, said method comprising the steps of:	Page 15, line 26 - Page 16, line 13; Figure 4 Figure 4 shows an active matrix liquid crystal display circuit. Data signals are supplied to liquid crystal layers through a plurality of thin film transistors 21, 22 arranged in a matrix of pixels. Gate lines and data lines (such as gate line 50 and data lines 52 and 53) are connected to each transistor.
forming a semiconductor layer on a substrate;	Page 16, line 27 - page 17, line 8; Figure 3A A semiconductor (silicon) layer is formed on substrate 1.
forming a gate insulating film on said semiconductor layer;	Page 21, lines 7-13; Figure 3B A gate insulating film 27 is formed on the semiconductor (silicon) layer as shown in Figure 3B.
forming a gate electrode above said gate insulating film and a gate line in electrical contact with said gate electrode;	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; Figures 3B and 4 Gate electrode 25 is formed above gate insulating film 27 (Figure 3B) and gate line 50 is formed in electrical contact with gate electrode 25 (Figure 4).
forming a source region and a drain region in said semiconductor layer by adding impurities thereto as donors or acceptors using said gate electrode as a self alignment mask;	Page 21, lines 2-6 and lines 19-24; Page 22, lines 6-11; and Page 37, line 29 - Page 38, line 5; Figures 3D Source region 35 and drain region 33 are formed in the semiconductor (silicon) layer by adding either boron (acceptor) or phosphorous (donor) impurities, using the gate electrode as a self-alignment mask.
simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line and simultaneously form a lateral offset, ΔL, from said source region and said drain region to the sidewalls of said gate electrode; and	Page 5, line 24 - Page 6, line 13; Page 6, line 22 - Page 7, line 4; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G As clearly illustrated in Figure 1 source and drain regions 3 are laterally offset by a distance L from each of the adjacent sidewalls of the gate electrode 8, which is covered with aluminum oxide 10. Similarly, in Figure 3G, source region 35 and drain region 33 both have a lateral offset from the side edges of gate electrode 25, which is covered by aluminum oxide layer 40 formed by anodic oxidation. As is further discussed with respect to the following clause of this claim, pages 6-7 state that the same anodic oxide film covers both the gate electrode and gate wiring. Therefore, this anodic oxide film formed on the gate electrode and the gate line is formed at the same time. The anodic oxidation process necessarily must reduce the dimensions of the gate electrode as stated, for example, in column 3, lines 44-55 of U.S. Patent 5,583,366.

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/841,644
forming a data line in electrical contact with said source region and crossing over said gate line at a cross-over location, wherein said overlying gate insulator is located between said data line and said gate line at said cross-over location to insulate said data line from said gate line.	Page 6, line 22 - Page 7, line 4; Page 21, lines 14-18; and Page 24, lines 7-11; Figures 3B and 3G Data line 53 is coupled to thin film transistor 22, and crosses over gate line 50 at a cross-over location, as shown in Figure 4. Pages 6-7 of the specification supports this limitation by disclosing that "other wiring, e.g., a wiring for the source electrode, may be crossed over this aluminum oxide film to establish a three-dimensional wiring . . . ." (Emphasis added). Thus, the aluminum oxide film formed on the gate electrode is the same aluminum oxide film that insulates the gate electrode 50 from the source line 53, which crosses over the aluminum oxide. Since the aluminum oxide film is formed both on the gate electrodes 25, 26 and gate line 50, page 7 clearly discloses that another wiring, such as the source electrode wiring 53, crosses the gate line at a cross-over location.
24. The method of claim 23 wherein said gate electrode is comprised of tantalum, and wherein said overlying gate insulator comprises tantalum oxide.	Page 28, lines 5-8 and 21-31 Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
25. The method of claim 23 wherein said gate electrode is selected from the group consisting of tantalum and aluminum.	Page 21, lines 14-18, Page 22, lines 23-30, and Page 28, lines 5-8 and 21-31; Figures 3B and 3E As discussed on Pages 21 and 22, gate electrode 25 is formed from aluminum (Figure 3B). Aluminum oxide is formed around gate electrode 25 by anodic oxidation. Page 28 discloses that the gate electrode could be comprised of tantalum and discloses that anodic oxidation of the gate electrode is performed, which would necessarily result in tantalum oxide being formed.
26. The method of claim 23 wherein the semiconductor layer is a silicon layer formed by decomposing a silane gas using CVD.	Page 16, line 27 - Page 17, line 21 The semiconductor layer is silicon formed by decomposing monosilane, disilane, or trisilane using either plasma CVD or low pressure CVD.
27. The method of claim 23 wherein the semiconductor layer is a polysilicon layer formed by first forming an amorphous silicon layer and annealing the amorphous silicon layer at a temperature within a range of 450° C. to 700° C. for 12 to 70 hours.	Page 18, line 20 - page 19, line 18 As described on pages 18-19, a deposited amorphous silicon film is heated at a temperature of 450-700 °C for 12-70 hours to increase the crystallinity of the film.
28. The method of claim 23 wherein the gate insulating film is sputter formed on a surface of the semiconductor layer.	Page 16, line 31 - Page 17, line 16

PENDING CLAIMS	SUPPORT IN U.S. SERIAL NUMBER 08/841,644
29. The method of claim 23 wherein the source region and the drain region are formed by implanting phosphorous ions into the semiconductor layer through the gate insulating film.	Page 21, lines 22-29 Source 35 and drain 33 are formed from implanting phosphorous through gate insulating film 27.
30. The method of claim 29 wherein the implanted phosphorous ions are radiated with a laser to reduce the resistance level in the semiconductor layer.	Page 11, lines 8-20 and Page 30, lines 2-14 Page 11 and 30 disclose laser irradiation of source/drain regions including phosphorous to activate these regions and thus reduce the resistance level in the semiconductor layer.
31. The method as defined in claim 23 wherein the overlying gate insulator is formed having a lateral thickness, ΔI, which is greater than the lateral offset, ΔL.	Page 5, line 24 - Page 6, line 13; Page 21, lines 19-24; Page 22, lines 23-30; Figures 1, 3E and 3G During the process described with respect to the formation of the device, source region 35 and drain region 33 are formed before anodic oxide coating 40 is formed. The process described must necessarily result in a thickness of the oxide layer being greater than the lateral offset distance L between source and drain regions and the adjacent edge of the gate electrode. That is, since the source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized, the thickness of the oxide layer will inherently be greater than the lateral offset distance L.
32. The method as defined in claim 23 wherein the step of forming the overlying gate insulator by anodic oxidation decreases the width of the gate electrode by about twice the lateral offset, ΔL.	The claimed reduction in width of the gate electrode is an inherent result of the described process. That is, source and drain regions are formed using the gate electrode as a mask, and the gate electrode is subsequently anodically oxidized and reduced in width as discussed in connection with claim 1 above. Since the lateral offset is defined to be the distance from the source region and the drain region to the sidewalls of the gate electrode, and this distance is equal to the amount of reduction in the size of the gate electrode on either side, the gate electrode will necessarily be reduced by about twice the lateral offset, ΔL.